Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (original) A method for reducing the effects of spurious frequencies in a wireless communications device, the method comprising:

providing a plurality of selectable passband ranges for the wireless communications device;

selecting one of the passband frequency ranges;

determining a clock frequency that produces no substantial spurious signals in the selected passband frequency range;

adjusting a clock to generate a clock signal at the clock frequency; and,

driving a processor with the clock signal.

2. (original) The method of claim 1 further comprising:

providing a cellular passband frequency range and a PCS passband frequency range.

3. (original) A method for avoiding spurious frequencies in the transceiver passband of a wireless communications device, the method comprising:

generating a clock signal at a clock frequency, the clock signal having a plurality of harmonics, each harmonic having a harmonic frequency;

generating a transceiver carrier signal at a carrier frequency; and,

selecting the clock frequency so that none of the harmonic frequencies is substantially equal to the carrier frequency.

4. (original) The method of claim 3 wherein generating a transceiver carrier signal at a carrier frequency includes generating a transceiver carrier signal having a center frequency of approximately 900 megahertz (MHz);

the method further comprising:

initially generating a clock signal at a frequency of 19.2 megahertz (MHz) with a 46th harmonic at 883.2 MHz; and,

wherein selecting the clock frequency so that none of the harmonic frequencies is substantially equal to the carrier frequency includes increasing the clock frequency from 19.2 MHz to 26.24 MHz.

5. (original) A method for reducing the effects of clock harmonics in the passband of a wireless communications device, the method comprising:

generating a clock signal at a clock frequency, the clock signal having a plurality of harmonics, each harmonic having a harmonic frequency;

generating a transceiver carrier signal at a carrier frequency; and,

changing the clock frequency so that none of the harmonic frequencies is substantially equal to the carrier frequency.

6. (original) A method for reducing the effects of clock harmonics in the passband of a wireless communications device, the method comprising:

generating a microprocessor clock signal at a clock frequency, the clock signal having a plurality of harmonics, each harmonic having a harmonic frequency;

generating a transceiver carrier signal at a carrier frequency, wherein the clock frequency is not substantially equal to any of the harmonic frequencies;

changing the carrier frequency to a second carrier frequency, wherein the second carrier frequency is to be substantially equal to one of the harmonic frequencies; and

changing the microprocessor clock frequency to a new clock frequency wherein the new clock frequency does not have any harmonic frequencies that are substantially equal to the new carrier frequency.

7. (original) A system for reducing the effects of spurious frequencies in a wireless communications device, the system comprising:

a microprocessor having a reference frequency input;

a clock having an output connected to the microprocessor input, and an input for selecting clock frequencies;

a transceiver having a port to transceive a plurality of selectable communication passbands in response to selection commands received at an input; and,

wherein the clock frequency is selected to avoid harmonic frequencies in the transceiver passband.

8. (new) The system of claim 7 wherein the microprocessor comprises a programmable logic device.

9. (new) The system of claim 7 wherein the microprocessor comprises a gate array.

10. (new) A method for reducing the effects of spurious frequencies in a wireless communications device, the method comprising:

providing a plurality of selectable passband ranges for the wireless communications device;

selecting one of the passband frequency ranges;

determining a clock frequency that produces no substantial spurious signals in the selected passband frequency range;

adjusting a clock to generate a clock signal at the clock frequency; and,

driving a logic device with the clock signal.

11. (new) The method of claim 10 wherein the logic device is a programmable logic device.

12. (new) The method of claim 10 wherein the logic device is a gate array.

13. (new) A wireless communications device comprising:

a clock;

a processor configured to perform the following steps:

selecting one of a plurality of passband frequency ranges;

determining a clock frequency that produces no substantial spurious, and;

adjusting the clock to generate a clock signal at the clock frequency;

a transceiver coupled to the processor and configured to send and receive electromagnetic signals;

and,

an antenna coupled to the transceiver.

14. (new) The wireless communications device of claim 13 wherein the processor comprises a programmable logic device.

15. (new) The wireless communications device of claim 13 wherein the processor comprises a gate array.

16. (new) The wireless communications device of claim 13 wherein the transceiver comprises a receiver.

17. (new) The wireless communications device of claim 13 wherein the transceiver includes multiple transceivers.

18. (new) The device of claim 13 wherein:

the transceiver operates at a transceiver carrier frequency of approximately 900 megahertz;

the clock initially generates a clock signal at a frequency of 19.2 megahertz; and,

the processor increases the clock signal frequency from 19.2 megahertz to 26.24 megahertz;

19. (new) A wireless communications device comprising:

a clock capable of generating a clock signal at a clock frequency, the clock signal having a plurality of harmonics, each harmonic having a harmonic frequency;

a processor configured to perform the following steps:

causing a carrier frequency to be changed to a second carrier frequency, wherein the second carrier is substantially equal to one of the harmonic frequencies;

causing the clock frequency to change to a new clock frequency wherein the new clock frequency does not have any harmonic frequencies that are substantially equal to the new carrier frequency;

a transceiver coupled to the processor and configured to send and receive electromagnetic signals;

and,

an antenna coupled to the transceiver.

20. (new) The wireless communication device of claim 19 wherein the processor comprises a gate array.